AMENDMENT TO SPECIFICATION

Please amend the paragraph at page 2, lines 4-15 as follows:

[0005] Namely, at each data pin of the DDR SYNCHMOMORY, each of two continuous data is inputted or outputted at each of the rising and falling edges of the external clock signal. As a result, though a frequency of the external clock signal, i.e. generally an operating clock signal, does not increased, the DDR SYNCHMOMORY can have at least twice the bandwidth ~~more than~~as the SDR SYNCHMOMORY and operate in high speed ~~as much~~.

[0006] ~~In~~ On the other hand, for stabling an operation of the DDR SYNCHMOMORY, new configurations which do not exist in the conventional semiconductor memory device ~~is~~ are necessary. For example, these are a column address strobe (CAS) latency, a burst length, an additive latency, and the like.